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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,477	12/26/2001	Chang Gone Kim	2658-0279P	2997

2292 7590 02/22/2005

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EXAMINER	
AWAD, AMR A	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,477	KIM, CHANG GONE	
	Examiner	Art Unit	
	Amr Awad	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/17/2004 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 8, 11-12, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui (US patent NO. 5,784,039; hereinafter referred to as Yasui) and Applicant Admitted Art (figure 2 and its relevant text; hereinafter referred to as APA) in view of Kubota et al. (US patent NO. 5,754,155; hereinafter referred to as Kubota).

As to independent claim 1, Yasui (figures 1A, 1 B and 2) teaches a power sequence apparatus comprising: a power supply (the power supply for generating VG1 through VGm+1) for simultaneously generating a gate high voltage (VGH) and a gate low voltage (VGL) (col. 5, lines 32-62). Yasui (figures 2A, 3B, 4A and 4B) teaches a

device driving circuit sequentially outputting the gate high voltage (VGH) and then the gate low voltage to a device (VGL); and a voltage controller (the switch disposed between VGH and VGH shown in figures 3A and 313) for processing the gate high voltage using a plurality of switching circuits (as can be seen in figures 3A and 313; each gate line has its switch equivalent circuit) to supply the gate high voltage after the gate low voltage is supplied to the device driving circuit (col. 6, lines 7-67 and col. 9, lines 28-44).

Yasui does not expressly teach having the high and low voltage supplied simultaneously. However, APA (figure 2) shows simultaneously applying high and low voltages VGH and VGL (page 3, lines 16-27).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the teaching of APA having the VGL and VGH voltages simultaneously applied to be incorporated to Yasui's device so as to be able to synchronized the two voltage to be able to control the power supply sequence with ease without malfunction.

Yasui and APA do not expressly teach that the voltage controller disposed between the power supply and the device driving circuit.

However, Kubota (figures 1-2) shows a liquid crystal display device that includes Power supply circuit 11a, and a voltage control circuits (the voltage generating circuit 12a and the current supply circuit 13) disposed between the power supply and the device driving circuit (3) for supplying the VGH and the VGL to the driving circuit (col. 9, lines 12-19 and col. 9, lines 42-48).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the teaching of Kubota having a control circuit disposed between the power supply and the driving circuit to be incorporated to Yasui's device so as motivated by Kubota, to provide the same level of voltage to the driving circuit as the reference voltage of the input signal (col. 9, lines 45-48), and therefore, to provide an image display device which does not require manual adjustment of the driving voltage and bias voltage (col. 5, lines 41-44).

As to independent claim 8, the claim is substantially similar to claim 1 and would be rejected as shown above with respect to claim 1. The claim further includes the limitation of timing control part for generating a switching control signal. As can be seen in figures 3A and 313, Yasui shows the timing control shown by the controlling of switching between the high voltage gate and the low voltage gate based on the time period, which is fairly reads on the claimed limitation.

As to independent claim 12, the claim is substantially similar to claim 1 above except that claim 12 specifically recites that the device is part of a display panel that includes data driver. As can be seen in figure 1A, Yasui shows a display panel that includes a data driver (2) and a gate driver (3).

As to independent claim 17, the claim is substantially similar to claim 8 adding to it that claim 17 also recites a display panel with gate driver and data driver. As can be seen in figure 1A, Yasui shows a display panel with gate driver (2) and data driver (source driver 2).

As to claim 20, the claim is a method corresponds to apparatus of claim 1 and would be analyzed as previously discussed with respect to claim 1.

As to claim 11, as can be seen from figure 2, the switching is applied after a driving power is supplied to the power supply and after the gate low voltage is supplied from the power supply to the device driving circuit (col. 4, line 66 through col. 5, line 62).

4. Claims 2-7, 9-10, 13-16 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui, APA and Kubota in view of Lee (US Publication NO. 2001/0033266A1).

As to claims 2, 9, 13 and 18, as can be seen above with respect to claim 1, Yasui, APA and Kubota teach all the limitations of claims 2, 9, 13 and 18 except the citation of first switching circuit disposed between the power supply and the device driving circuit, and a second switching circuit connected between the first switching circuit and a gate output line of the power supply.

However, Lee (figure 5) teaches an active matrix liquid crystal display that includes a voltage controller (46), low level gate voltage generator (40), high level voltage generator (44), first switch (39) connected between the power supply and the device driving circuit and a second switch (50) connected between the first switch and a gate low level voltage (page 4, paragraph NO. 37).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the teaching of Lee having two switching circuits arranged in the described manner, to replace the circuit of Yasui so as motivated by

Lee, to eliminate flickering and residual images with a simplified circuit configuration (page 2, paragraph N0. 11).

As to claims 3 and 14, Lee (figure 7) shows a first resistor (R1) and a capacitor (C1) connected in parallel to the second switch (50) for switching the second switch according to a RC time constant (page 4, paragraph NO. 39), the second resistor (R2) shown in figure 10 connected between the second switching (50) and a ground voltage can be easily combined to figure 7 so as to be able to prevent a leakage of voltage to be charged (page 5, paragraph NO. 41).

As to claim 4, as can be seen above with respect to claim 3, Lee shows RC circuit (R1 and C1) connected between the second switching (50) and the power supply. As to claim 5, it is apparent from figures 4 and 7 of Lee's the whole device is build on a single substrate which makes it obvious that the two switches are integrated into a single chip.

As to claims 6 and 15, the claims are broad enough that the wiring between the first and second switch in figure 5 of Lee's device can be considered the resistor which connects the first and the second switches.

As to claims 7, 10, 16 and 19, the transistor (MN) in figure 9 of Lee's device is part of the second switch.

Response to Arguments

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lee (US patent NO. 5,940,055) teaches a liquid crystal display with row-selective transmittance compensation and methods of operation thereof.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amr Awad whose telephone number is (703)308-8485. The examiner can normally be reached on Monday through Fridary from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkwitz can be reached on (703)306-0403. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A. A.

AMR A. AWAD
PRIMARY EXAMINER